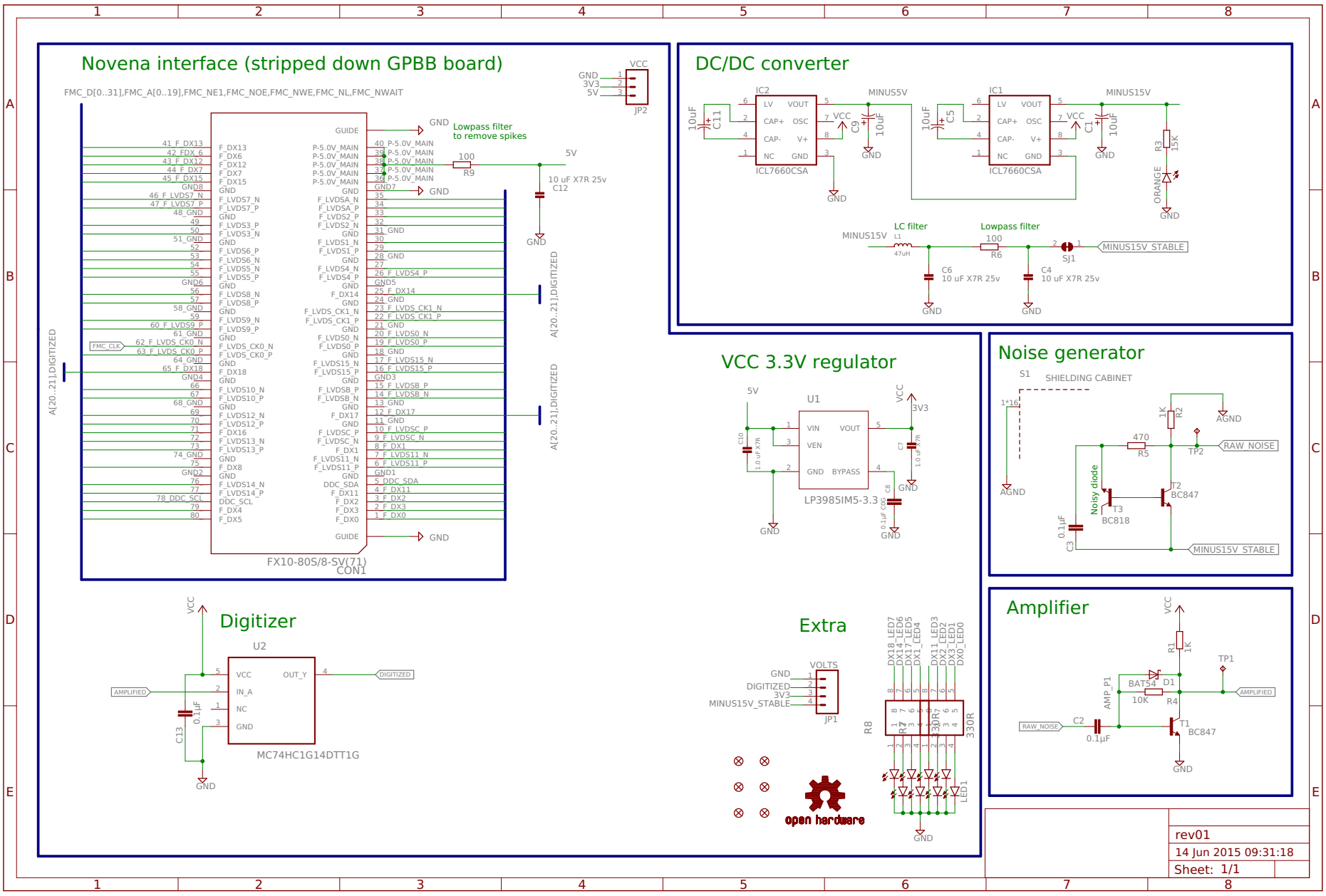
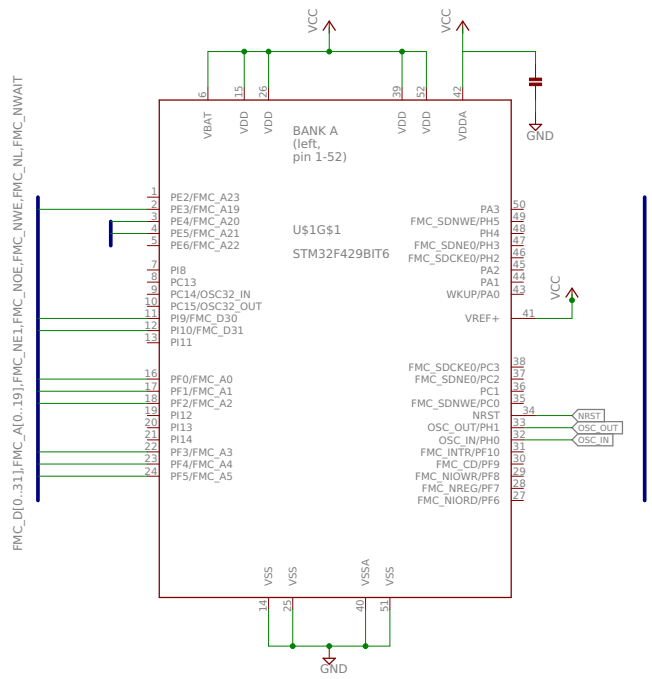
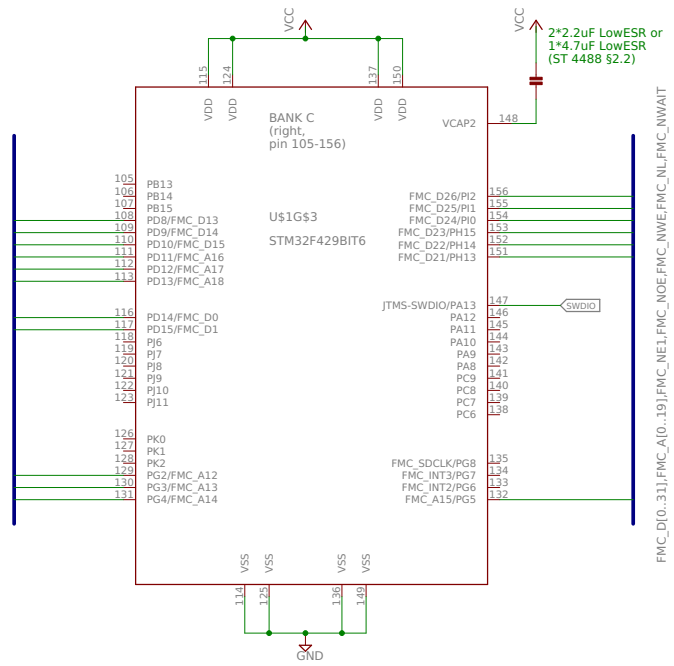
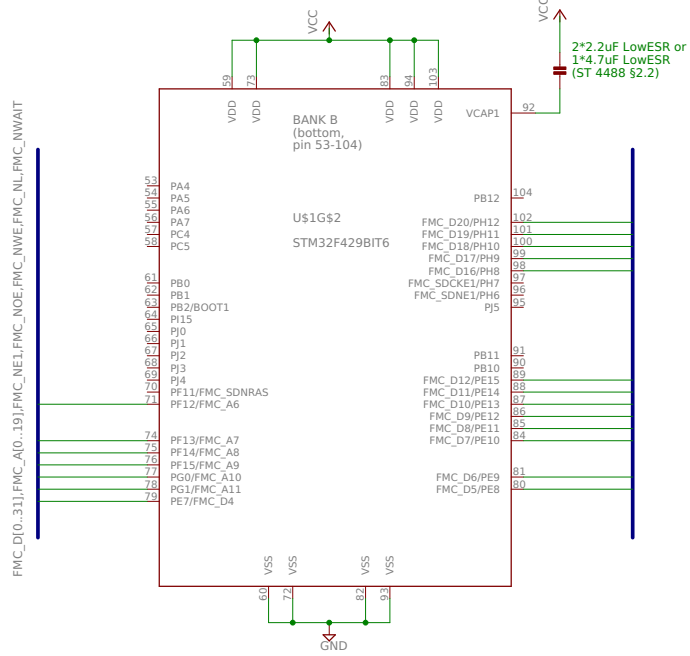
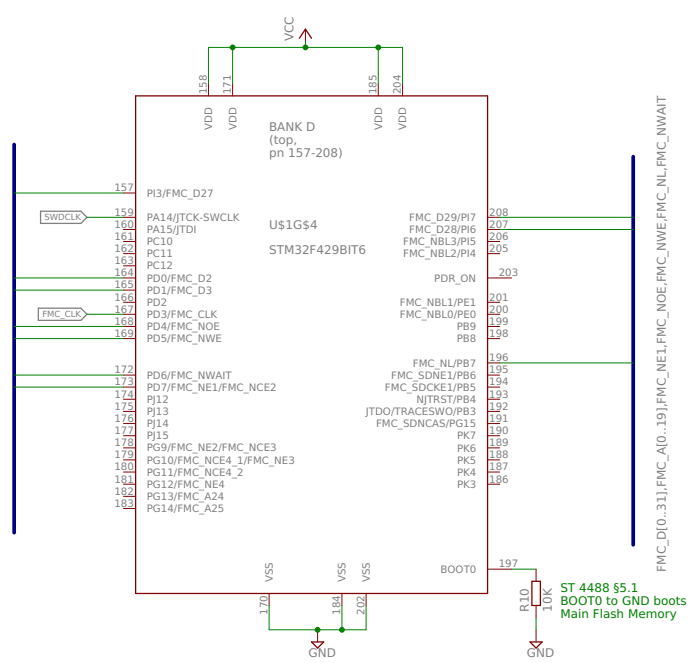
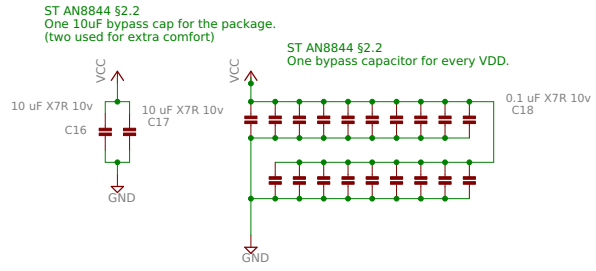

Novena interface (stripped down GPBB board)
FMC_D[0..31],FMC_A[0..19],FMC_NE1,FMC_NOE,FMC_NWE,FMC_NL,FMC_NWAIT
FX10-80S/8-SV(71)
CON1
Lowpass filter to remove spikes
DC/DC converter
ICL7660CSA
LC filter
Lowpass filter
MINUS15V_STABLE
VCC 3.3V regulator
LP3985IM5-3.3
Noise generator
SHIELDING CABINET
RAW_NOISE
Noisy diode
Amplifier
AMPLIFIED
Digitizer
MC74HC1G14DTT1G
Extra
open hardware
rev01
14 Jun 2015 09:31:18
Sheet: 1/1

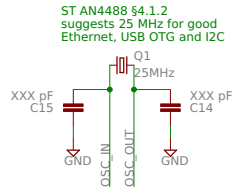

BANK A
(left,
pin 1-52)
U$1G$1
STM32F429BIT6

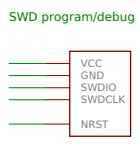

BANK C
(right,
pin 105-156)
U$1G$3
STM32F429BIT6
2*2.2uF LowESR or
1*4.7uF LowESR
(ST 4488 §2.2)


BANK B
(bottom,
pin 53-104)
U$1G$2
STM32F429BIT6
2*2.2uF LowESR or
1*4.7uF LowESR
(ST 4488 §2.2)


BANK D
(top,
pn 157-208)
U$1G$4
STM32F429BIT6
ST 4488 §5.1
BOOT0 to GND boots
Main Flash Memory


ST AN8844 §2.2
One 10uF bypass cap for the package.
(two used for extra comfort)
ST AN8844 §2.2
One bypass capacitor for every VDD.


ST AN4488 §4.1.2
suggests 25 MHz for good
Ethernet, USB OTG and I2C


SWD program/debug